ELECTRICAL SHIELDING IN STACKED DIES BY USING CONDUCTIVE DIE ATTACH ADHESIVE

The invention relates to electronics packaging. More particularly the invention relates to the use of conductive die attach adhesive to provide electrical shielding in an array of stacked integrated circuit devices.

As integrated circuit technology improves to increase the density and complexity of devices that may be rendered in a given area of substrate, a significant challenge is posed to the packaging of these devices. In computer applications, for example, the width of the data bus has increased from 16, 32, 64, to 128 bits and beyond. During the movement of data in a system it is not uncommon for a bus to have simultaneously switching outputs (SSOs). The SSOs often result in the power and ground rails of the chip experiencing noise owing to the large transient currents present during the SSOs. If the noise is severe, the ground and power rails shift from their prescribed voltage causing unpredictable behavior in the chip.

As the technology evolves, a trend of miniaturization and a drive towards Multi Chip Modules (MCM) and System in Package (SIP) can be observed. These trends bring in a move towards three-dimensional (3D) packaging, that is, the stacking of multiple device dies on top of one other.

A significant challenge in the stacking of multiple device dies is the possibility of electrical interference among them, especially in situations in which analog and digital devices are combined or if one of the device die is a high frequency device, the interference created may cause devices to malfunction. There is a need to prevent electrical interference in packaged devices having multiple device dies stacked on one another. A way to minimize electrical interference is to make robust the grounding between the device dies and the package. The present invention provides a structure and method for achieving grounding between stacked dies and the package

An integrated circuit (IC) device assembled in a package (5) having a plurality of die including a first device (20) and at least one additional device (30), the IC comprising

In an example embodiment, there is an integrated circuit (IC) device assembled in a package having a plurality of die including a first device and at least one additional device. The IC comprises a substrate. A first device die, having bonding pads including ground connections, is die attached to the substrate. An additional device, having bonding pads including ground connections is disposed on top of the first device. The additional device is die attached to the first device. The ground connections of the first device are coupled to

the ground connections of the additional device. A feature of this embodiment, is that the ground connections of the first device are connected to the ground connections of the additional device with a conductive adhesive.

In another example embodiment, there is a method for packaging an integrated circuit (IC) having a plurality of die including a first device and at least one additional device, and having a grounded substrate.. The method comprises attaching a first device onto a substrate, the substrate ground connections. On the first device, an insulating material is applied. The additional device die is attached onto the insulating material. At predetermined ground connections, the first device die is bonded to the second device die. The predetermined ground connections are then bonded to the substrate ground connections. A feature of this embodiment is that the bonding of the first device to the additional device at predetermined ground connections includes: using at least one of the following: conductive adhesive, a solder re-flow, and a conductive interposer.

The above summaries of the present invention are not intended to represent each disclosed embodiment, or every aspect, of the present invention. Other aspects and example embodiments are provided in the figures and the detailed description that follows.

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 depicts in side view, bonding of two device die in accordance with an embodiment of the present invention;

FIG. 2A is an example pad layout for a die to be packaged;

FIG. 2B illustrates an example pad layout having grounding pads for use in an embodiment according to the present invention;

FIG. 3 depicts in top view, an example of two die stacked and bonded together according to an embodiment of the present invention;

FIG. 4 depicts in top view, an example of an alternative placement of grounding pads according to an embodiment of the present invention;

FIG. 5A illustrates in top view of stacked die in an example embodiment according to the present invention;

FIG. 5B is a cross-section of the example of FIG. 5A;

FIG. 6 illustrates, in side view, the stacking two same-sized die in an example embodiment according to the present invention;

FIG. 7 depicts the stacking of two die in an example embodiment according to the present invention;

FIG. 8 illustrates the use of a cross bar grid to connect ground pads together in example embodiment according to the present invention;

FIG. 9 illustrates using straps to connect grounds together in accordance with another embodiment of the present invention; and

FIG. 10 depicts an assembly process flow for a two-stacked die array in accordance with an embodiment of the present invention.

The present invention has been found to be useful in the assembly of electronic circuits having multiple die stacked on top of one another. The grounding areas of the multiple die are coupled together enhancing the integrity of ground in the electronic circuits. In grounding selected device pads in a multiple die assembly, it will be appreciated that the term grounding may applied to those regions on a device or package that are connected in common, such as power supply nodes. These power supply nodes may be at zero, positive, or negative volts. For example, in some CMOS devices there may be multiple power supply rails, such as zero volts (ground), =1.2v, 3.3v, 5.0v, *etc.* In modern packaging is it not uncommon to have multiple power supply nodes, including those for ground.

In an example embodiment according to the present invention, in a ball grid array package (BGA) at a ball location is coupled to a grounding location for a pair of die stacked on top of each other. Referring to FIG. 1, a package assembly 100 includes a substrate 105 with a ball assembly 145 providing electrical connection to a package-bonding pad 140 through conductive traces (not illustrated). A first die 120a is attached to the substrate 105 with an adhesive 110. The adhesive may be both film and liquid. Alternatives to adhesive may include soldering or eutectic die attach. Placed on top of the first die 120a is a second die 120b. The dies 120 are electrically coupled via a conductive adhesive 115. The circuit may be designed so that the second die 120b is smaller in area by predetermined amount than that of the first die 120a and that there is accommodation made in the first die 120a for placement of the second die 120b. The accommodation may include, but is not limited to, electrical bond pads to couple the underside of the second die 120b to the first die 120a. An insulating film may be placed between with two die with appropriate openings defined therein to only allow the conductive adhesive 115 to bond in regions in which electrical contact is desired. Bond wires 125 couple ground pads on dies 120 to bonding pad 140. In

a completed package assembly 100, a molding compound 135 seals the electrical circuit from the outside environment.

In another example embodiment, the second die 120b may have a metallization applied to the underside to enhance the conductivity of the ground connection facilitated by the conductive adhesive. Such metallization would likely be applied during the latter stages of wafer fabrication, after completion of the final topside passivation.

Referring to FIGS. 2A and 2B. Die 200 has an arrangement of bond pads 210. In applying an embodiment of the present invention, during the design and layout process, the circuit 205 may be arranged to have interior pads 205 connected to ground in the core area of the die, as well as the typical bond pads 215. The interior pads 205 may be laid out to make optimum use of the core area. The interior pads 205 locations may be at the center (as illustrated in FIG. 2B) or be offset from the center at appropriately defined areas.

Referring to FIG. 3, in an example embodiment, on a device die 300, the grounding pads 325 are located near the bond pads 310. Layer 327 is an insulating mask that exposes the grounding pads 325 but protects the die 300 from unintended ground connections after the application of a conductive adhesive 449 such as shown in FIG. 4A.

Referring to FIG. 4, in an example embodiment, a device die 305 has the grounding pads 335 located at the corners of the core area near the bonding pads 310.

Referring to 5A, in an example embodiment, the device 400 has grounding pads 445 located at the corners of the bonding pads 410. In a partial view, an insulating mask 447 has openings for the grounding pads 445. Upon the insulating mask 447, the conductive adhesive 449 is applied. A cross-section at the "A" dashed-line is depicted in FIG. 5B. In this example, areas of the second die, stacked upon the first die, are comparable. The bonding pads 410 may be bonded via wire bonds, tape, or other suitable connection that can undergo stress of placing the insulating mask 447 thereon. The resulting structure is a sandwich of two similarly sized device die.

If the passivation is sufficiently impermeable, the conductive adhesive may be directly applied to the first die to electrically couple the second die's grounding to that of the first die.

Referring to FIG. 6, in an example embodiment, two die of the same size may be joined together according to the present invention. In a BGA package 5, two die are mounted on a BGA substrate 10. The balls 15 connect to bonding pads via circuit traces (not illustrated) in the substrate 10. A first die 20 of a given size has a conductive

interposer 25 applied to its surface. The conductive interposer 25 may have conductive adhesive to bond the two die to one another. The stiffness of the interposer 25 prevents the second die from squishing the bond wires 35a of the first die. The second die 30 is attached to the conductive interposer 25. Bond wires 35a connect the first die 20 and bond wires 35b connect the second die 30 to the BGA via package bonding pads. The interposer 25 provides sufficient clearance for the first bond wires. After the two die are wire bonded, the assembly is sealed with an encapsulating compound 40.

Referring to FIG. 7, in an example embodiment according to the present invention, a circuit device 500 has two die stacked upon each other. A first die 505 has bonding pad ring 510. Grounding pads 515 are situated about the center of the first die 505. A second die 520, on its underside, is attached to the grounding pads 515 with a conductive adhesive. The second die 520 is smaller than the first die 505. The bond pads 525 may be arranged so as to facilitate both the wire bonding of the first die's 505 bonding pads 510 and the second die's 520 bonding pads 525. There may be an insulating mask placed upon the first die 505 if it is likely that the conductive adhesive may make unintended connections to ground.

Referring to FIG. 8, in an example embodiment, in place of grounding pads 515, a conductive grid 530 may be laid across the die and be coupled to bonding pads defined as ground. The defining of grounded bonding pads may be part of the device's design process. The second die 520 on its underside may then be bonded with conductive adhesive to couple the second die 520 to the ground. The conductive grid 530 may a suitable conductor, such as copper, aluminum, gold, silver, and alloys thereof. Cost and process dictate which metal is suitable. Furthermore, the coefficient of thermal expansion (CTE) is a important to material choice in that materials chosen should have similar CTE. Dissimilar CTE of the materials that build a package would ultimately lead to premature mechanical failure.

Referring to FIG. 9, in another example embodiment, a device 600 may have a first die 905 and a second die 945 coupled together at ground a designated bonding pads 920a, 920b, and 920c chosen from the bonding pads 910a, 910b, and 910c. In this example, the first die 905 may have staggered bond pads in two rings, pads 910a and pads 910b. As mentioned earlier, these grounding pads would be designated during the design phase of the first die 905 and the second die 945. Conductive straps 930a, 930b, and 930c couple the electrical grounding of die 905 and 945 by their connection to grounded bonding pads 920a, 920b, and 920c. Sample, pad landings 960 connect the bonding pads 910a, 910b, 910c with

bond wires 955. A number of these pad landings 960 are defined as ground. These multiple connections make for a robust ground. Likewise, in another example embodiment, the present invention may be used to make robust power connections. Having both robust ground and power connections reduces the multi-chip device's susceptibility to noise, such as ground bounce during bus switching.

Referring to FIG. 10, in an example embodiment, there is a process 1000 for assembling a package having two or more device die. The user selects a suitable substrate 1005 having a landing upon which a die may be attached. Paste or other suitable adhesive 1010 is dispensed on the landing and a first die is attached 1015. To adhere the die securely, a snap curing or oven curing 1020 is performed. This curing stabilizes the adhesive, to prevent the die from moving. Since the adhesive is conductive, the user is able to couple the ground of the first die with that of the additional die. For the first insulating layer, a suitable film is cut to predefined dimensions and laminated 1025 on the die Typically the wafer is laminated with an adhesive tape. A second die is attached 1030 by similar steps outlined earlier In case a film die attach is used, the second die attach is only a die placement. Following the second die attach 1030, the package undergoes a film curing 1035. The second curing step is to cure the die attach compound and make sure the second die is fixed, so it does not shift in later processing. The package having two die attached undergoes a plasma cleaning 1040. Plasma cleaning is organically cleaning the module so as to make the bond pads free of organic contamination. If there are additional die to attach 1045, the process is repeated from 1030 through 1040. Otherwise, the assembly having at least two die, undergoes wire bond 1050. After wire bond 1050, the assembly goes through an additional plasma cleaning 1055. Having cleaned the assembly, the multiple dies are encapsulated in a molding compound 1060. Being a ball grid array package the balls are placed in the predetermined locations 1065. Depending on what ball count and ball pitch, JEDEC defines certain industry guidelines that need to be incorporated. In manufacturing, balls may be placed where desired. The most common way to do ball attach is to have a predefined pattern on a stencil. The balls will then be placed all at once from the stencil pattern defined on the substrate. After ball placement 1065, singulation 1070 is performed. Parts are typically processed in strip form, having a number of parts are in a strip. This strip is the carrier used to guide the parts through assembly. Typically all indexing holes used for positioning the parts at each machine are in the strip. During the singulation step, the BGA parts are milled, stamped or sawn out of it strip. Having completed the packaging, the

assembled package is marked 1075. Before, shipping to the end user the multiple-die device is tested 1080. Such testing is performed on ATE with hardware and software suitable for the multiple-die device. Although the aforementioned example covers BGA. Package, the process may be modified for use ed in lead frame packages, *etc.*

While the present invention has been described with reference to several particular example embodiments, those skilled in the art will recognize that many changes may be made thereto without departing from the spirit and scope of the present invention, which is set forth in the following claims.